A balanced millimeter wave doubler based on pseudomorphic HEMTs.

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Abstract

A balanced HEMT doubler for operation at millimeter waves has been analyzed, fabricated and characterized. Particular attention has been paid to the influence of the output circuit on the performance of the doubler. The doubler was analyzed with a harmonic balance method and experimentally an output power of 4dBm at 42 GHz was obtained. The conversion gain is approximately -1 dB at 40 GHz at an input power of 5dBm. Bias and frequency response were very close to the predicted ones.

Introduction

The use of a doubler could be a convenient way to overcome the problems associated with signal generation at millimeter wave frequencies. Several different doubler configurations are known from previous investigations [1,2,3]. The balanced doubler is especially attractive due to the high conversion efficiency and the effective suppression of the fundamental and the third harmonic frequencies [1,3]. The input signal to the doubler is fed to a power divider which divides the power equally between port 1 and 2 with 180° phase difference between the ports. The signals from the dividers are connected to a HEMT amplifier each, which are biased for clipping at the drains (fig. 1).

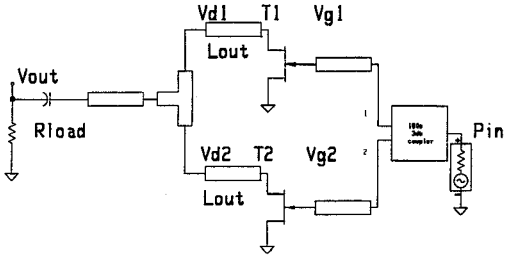

Fig. 1: Block diagram of the doubler.

The drains are connected by transmission lines. At the output, the fundamental and other odd harmonic signals have opposite phase and destructive interference cancel these frequency components. On the contrary, the second harmonic frequency signals have the same phase and therefore interferes constructively. By proper construction of the doubler conversion gain can be obtained. We present a 20 to 40 GHz doubler based on this principle.

Modeling of the HEMT and optimization of the doubler circuit

For the nonlinear simulation we have used a newly developed HEMT model [4] which is suitable for commercial harmonic balance simulators. The drain current dependence for the HEMT is expressed in accordance with previous MESFET models as $I_d[V_g,V_d]=I_{dA}[V_g].I_{dB}[V_d]$, where the first term is dependent only on the gate voltage and the second only on the drain voltage. The complete equation for the new model is:

$$I_{ds}=I_{pk}\cdot(1+\tanh(\psi))\cdot(1+\lambda V_d)\cdot\tanh(\alpha V_d),$$

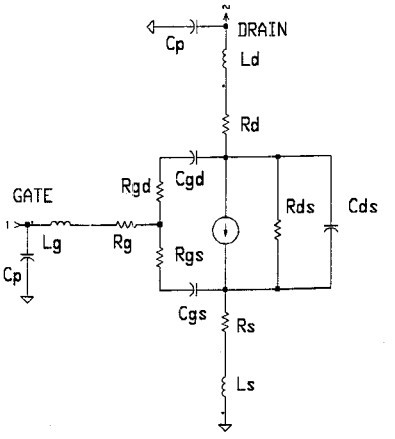

Fig. 2: Equivalent circuit of the transistor.

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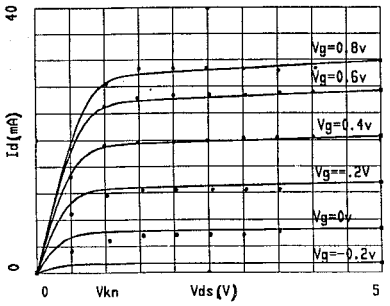

Fig. 3: Measured (dots) and simulated (line) I_d-V_d characteristics.

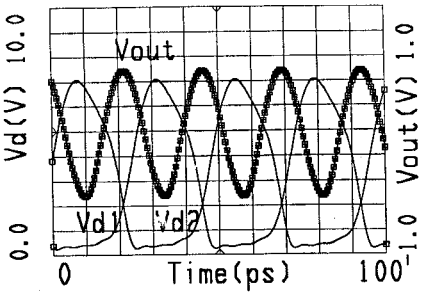

Fig. 4: Simulated output voltage.

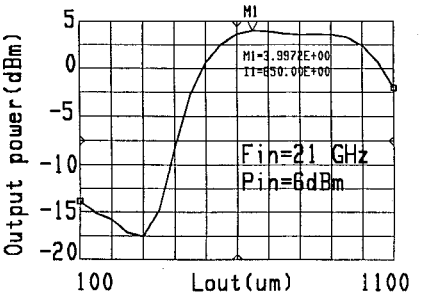

Fig. 5: Output power versus. L_{out}.

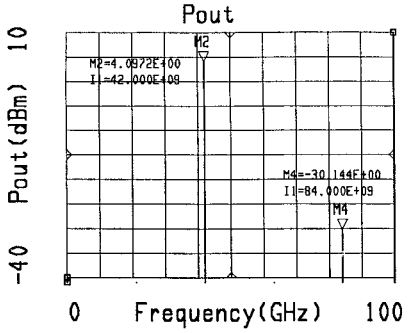

Fig. 6: Simulated output spectrum of the doubler

where I_{pk} is the current at maximum transconductance, Ψ is in general a power series function centred at the gate voltage for maximum transconductance, V_{pk}, and with variable V_g i.e.

$$\Psi=P_1(V_g-V_{pk})+P_2(V_g-V_{pk})^2+P_3(V_g-V_{pk})^3+....$$

where λ is a parameter influencing the dependence of the output conductance on V_d, α is the saturation voltage parameter influencing the linear part of the I_d vs V_d characteristics of the transistors. Parameters α and λ are the same as in Statz and Curtice model and

$$P_1= g_{mpk}/(I_{pk}(1+\lambda\cdot V_d))\sim g_{mpk}/I_{pk}$$

In our model a third term P_3 is used to improve the fitting of the drain current and g_m at voltages close to pinch off. The model was easily implemented in a commercial software, MDS from Hewlett Pacard, as a custom defined model. The parameters of the equivalent circuit (Fig 2) of the transistor which were obtained from measured S-parameter up to 62.5 GHz and DC-measurements are listed in Table 1. In Fig. 3 the measured and simulated I_d-V_d characteristics of the HEMT are shown.

Different modifications of the output circuit were investigated by using the harmonic balance method for a relatively small number of harmonics (typically 8-10). After the determination of the harmonic content, the voltages and the currents can be restored by an inverse Fourier transform. The HEMT drain voltages, and output voltage V_{out} are plotted in Fig. 4.

The effect of output transmission line lengths, impedances and DC bias circuits were investigated:

Short lengths of L_{out} ($L_{out}/\lambda_{out}<0.1$) results in a drop in multiplier efficiency (fig.5).

Optimum characteristic and best harmonic content of the doubler were obtained for an output circuit line, L_{out}, with a length approximately equal to $\lambda_{out}/4$. This length decouples the transistors at the first harmonic. and matches them for the second harmonic. Harmonics of higher order are 23 dB below the second harmonic output signal (fig. 6).

The analysis showed that the choice of the DC mode is not critical for the operation of the HEMT doubler. Nevertheless, from the point of view of optimization of the high frequency multiplier efficiency from the first to the second harmonic, optimization of output power, gain, dissipated DC power, spectrum contents, etc., the optimum mode is with a drain current $I_d=I_{pk}$. For maximum output power,

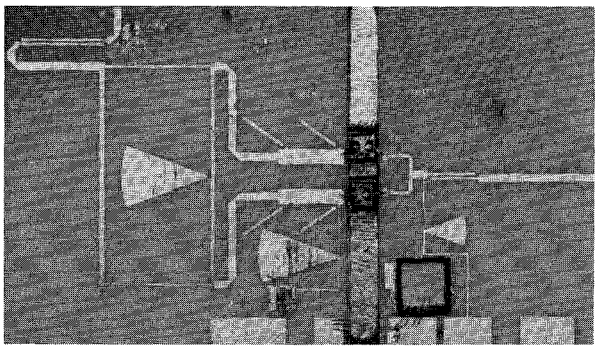

Fig. 7: Photo of the doubler circuit.

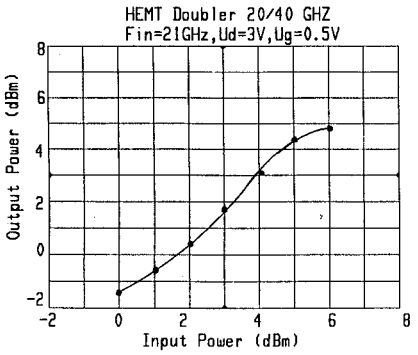

Fig. 8.Measured output power versus input power

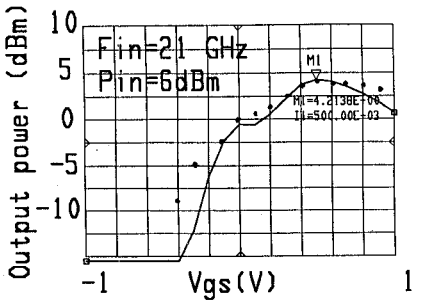

Fig. 9: .Measured output power vs gate bias.

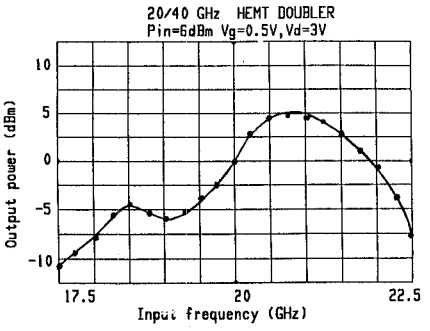

Fig. 10:Measured frequency response of the doubler

which were obtained for an input power of about 3-4 mW, the second harmonic output voltage V_{pk2} is approximately equal to the difference between the operating DC voltage V_{dc} and the knee voltage, V_{kn}, of the VA curve, $V_{pk2}=0.4(V_{dc}-V_{kn})$ (fig 3). An important point, often overlooked, is that the drain voltage can reach dangerously high levels, that could cause breakdown in the transistor.

The used software puts no particular limitation on the model used for the capacitance of the FET (linear, junction, Statz). In most cases however, the use of simple models is imperative. An analysis of the effect of the non-linearity of these capacitances on the frequency transformation processes has hence been carried out. The result of the analysis show that the differences are small (<10%) and for most cases the capacitances may be considered to be constant. This is because the main process responsible for the multiplication in the balanced doubler is the current clipping.

The relative importance of unbalance in the input power divider was also investigated: A 10^{o} phase deviation from the ideal 180^{o} phase difference or a 0.3 dB unbalance of the amplitude in the input circuit will decrease the output power 1 dB. With an unbalance in both amplitude (0.3 dB) and phase (10^{o}), results in a decrease of the output power of approximately 3 dB.

Experimental results

A photo of the doubler circuit is shown in Fig 7. The modeled doubler circuit was realized on 5 mil alumina substrate. ∂-doped pseudomorphic HEMTs with f_{max} of the order of 180 GHz were fabricated in our laboratory. The use of ∂-doping allows an undoped spacer layer in between the gate and the two dimensional electron gas channel, which has the important effect of increasing the gate breakdown voltage. 180^{o} phase difference of the input signals over a wide frequency band is required for realisation of a balanced doubler. A 180^{o} rat race hybrid was chosen for the experimental verification. The characteristic impedance of the individual elements of the hybrid were optimized for bandwidth. The values of the individual matching elements of the input circuits were found with a standard optimization program. They were further adjusted by the MDS (Hewlett Pacard) on the basis on the direct improvement in the multiplier efficiency for the second harmonic.

The drain voltage is applied through a common high impedance line, $\lambda_{out}/4$ long at the output frequency. Input and output to the doubler were made with V-connectors.
In Fig. 8, the output power from the doubler is plotted versus the input power. In the power measurement, the fundamental frequency component was effectively suppressed by using a WR-22 coaxial-waveguide transition at the output. The conversion gain is approximately -1 dB at 40 GHz with an input power of 5 dBm. The effect of bias is shown in fig. 9 where the simulated response is also plotted. The measured frequency response of the doubler is shown in fig. 10. Bandwidth is limited mainly by the input 180° rat race coupler. By using couplers with better characteristics [6,7] it should be possible to improve flatness of the output power versus.frequency response.

Conclusions.

A newly developed large signal HEMT model was applied for the analysis of a balanced HEMT doubler. An experimental investigation confirm the result of the harmonic balanced simulations. An output power of 4 dBm at 42 GHz was obtained experimentally, bias and frequency response were very close to the predicted ones.

Acknowledgement

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Table 1:Extracted parameters of the pseudomorphic HEMT.

R_g [Ω]	R_{gs} [Ω]	R_s [Ω]	R_f [Ω]	R_d [Ω]	R_{ds} [Ω]	C_{ds} [fF]	C_{rf} [fF]	C_{gs} [fF]	C_{gd} [fF]
8	5	5	9	6	1000	14	50	40	13

I_{pk} [mA]	P_1	P_3	V_{pk} [V]	λ	α
15	2.6	7	0.20	0.015	3

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